

Building Blocks for Millimeter-Wave Signal Sources

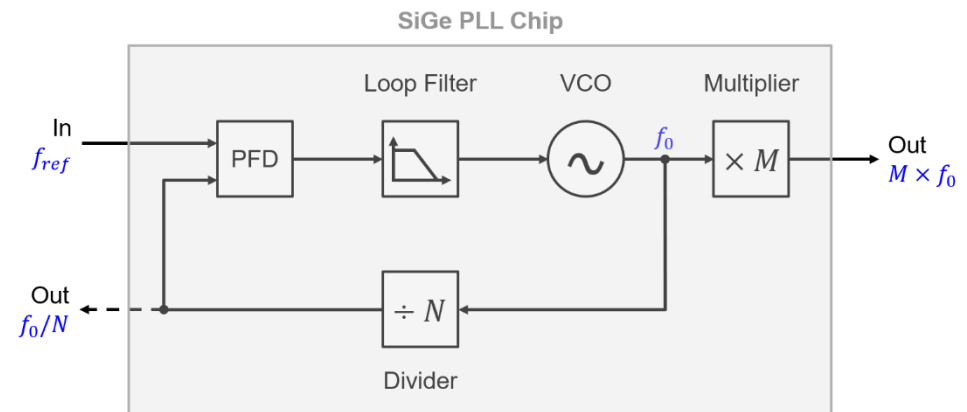
A key component in millimeter-wave (mmW) transceivers is the signal source, which is usually realized as a phase-locked loop (PLL). As the frequency increases, it gets more challenging to design on-chip signal sources with sufficient output power, adequately low phase noise and a wide tuning range, because of limited transistor gain, reduced quality factors and the rising impact of parasitics.

The aim of this thesis is to analyze and design a part of the signal source for emerging mmW applications. Depending on the thesis type (BA/MA), different topics are possible:

- PLL System Modeling and Behavioral Simulations
- Design of one of the building blocks (e.g. Frequency Divider, Frequency Multiplier, VCO, ...) in a SiGe BiCMOS Technology

Task:

- Theoretical Analysis of PLL models or circuit concepts, respectively
- Design and Simulation of the circuits in a state-of-the-art SiGe BiCMOS technology with industry-standard RFIC Design Tools (ADS, Cadence Virtuoso)



Requirements:

- Good understanding of circuits (e.g. ES, RFE or RFICS)

Language: German or English

Contact

M.Sc. Matthias Möck
Building 30.10, Room 1.32
E-Mail: matthias.moeck@kit.edu

Prof. Dr.-Ing. Ahmet Cagri Ulusoy
Building 30.10, Room 3.28
E-Mail: cagri.ulusoy@kit.edu