

## Building Blocks for High Speed Optical PAM-4 Receivers

Increasing data rates in electro-optical data transmission raise the demand for complex receiver architectures with high symbol rates. Additionally the data rate is enhanced by using modulated signals with multi bits per symbol. Here we will focus on PAM-4, 2 bits per symbol.

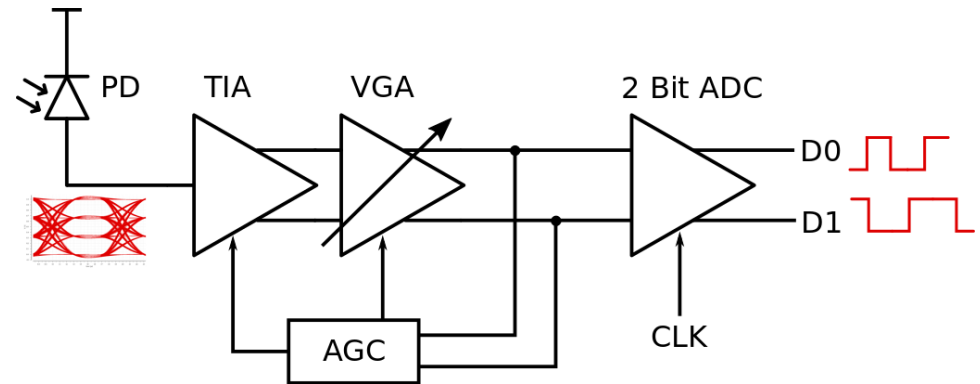
The receiver incorporates several building blocks like a transimpedance amplifier (TIA), variable gain amplifier (VGA), automated gain control (AGC) and a 2 bit ADC.

Goal of this thesis is a part of this receiver system with a symbol rate of 100 GBaud/s.

Several circuit architectures are investigated analytically and with simulation tools.

### Tasks

- Circuit design and simulation in a SiGe BiCMOS technology with industry standard RFIC design tools (Cadence Virtuoso, Keysight ADS)
- Layout and evaluation of parasitics (Post-Layout simulation, EM-simulation)
- The thesis will focus on a specific part of the complete system



### Contact

**M.Sc. Christian Bohn**  
Building 30.34 (LTI), Room 120  
E-Mail: [christian.bohn@kit.edu](mailto:christian.bohn@kit.edu)  
Phone: 0721-608 45102